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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,419	10/16/2003	Oh-Nam Kwon	8733.874.00-US	5831

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EXAMINER	
NGUYEN, HOAN C	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,419	KWON ET AL.	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I (claims 1-10) in the reply filed on 02 June 2005 is acknowledged.

Claims 11-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 02 June 2005.

Specification

The disclosure is objected to because of the following informalities: the specification does not disclose the feature "the data line, the source electrode, the drain electrode and the storage metal layer are all formed of a single layer of copper (Cu)" in claim 8. However, the specification ONLY disclose:

> [paragraph 53] The storage metal layer 218 may be formed with the data line 212 in the same process, and it can be Cu/Mo-alloy double layers or a Cu single layer.

This paragraph 53 disclose ONLY the storage metal layer (not the data line, the source electrode or the drain electrode) can be Cu/Mo-alloy double layers or a Cu single layer. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Maeda et al. (US6468822B2).

Maeda et al. teaches an array substrate for use in a liquid crystal display device comprising:

- a gate electrode 1 and a gate line, each having a molybdenum alloy (Mo-alloy) layer (first layer 1a) and a copper (Cu) layer (second layer 1b) configured sequentially on a substrate (col. 7 lines 14-25);
- a gate insulation layer 3 on the substrate to cover the gate electrode and the gate line;
- an active layer 4 arranged on the gate insulation layer in a portion over the gate electrode;
- an ohmic contact layer 5 on the active layer;
- a data line inherently on the gate insulation layer, the data line crossing the gate line and defining a pixel region;
- source and drain electrodes 6/7 on the ohmic contact layer, the source electrode (Fig. 3 shown) extending from the data line, and the drain electrode spaced apart from the source electrode;

- a passivation layer 10 on the gate insulation layer covering the data line and the source and drain electrodes, the passivation layer having a drain contact hole 9 exposing a portion of the drain electrode; and
- a pixel electrode 11 configured on the passivation layer in the pixel region, the pixel electrode electrically contacting the drain electrode through the drain contact hole.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3, 4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Chae (US6861368B2).

Chae teaches an array substrate for use in a liquid crystal display device comprising:

Claim 1:

- a gate electrode 160 and a gate line 162, each having a molybdenum alloy (Mo-alloy) layer 160a and a copper (Cu) layer 160b configured sequentially on a substrate;
- a gate insulation layer 150 on the substrate to cover the gate electrode and the gate line;
- an active layer 170 arranged on the gate insulation layer in a portion over the gate electrode;

- an ohmic contact layer 170b on the active layer;
- a data line on the gate insulation layer, the data line crossing the gate line and defining a pixel region;
- source and drain electrodes 176/178 on the ohmic contact layer, the source electrode 176 (Fig. 4 shown) extending from the data line, and the drain electrode spaced apart from the source electrode;
- a passivation layer 152/154 on the gate insulation layer covering the data line and the source and drain electrodes, the passivation layer having a drain contact hole 182 exposing a portion of the drain electrode; and
- a pixel electrode 188 configured on the passivation layer in the pixel region, the pixel electrode electrically contacting the drain electrode through the drain contact hole.

Claim 3:

- a storage metal layer (gate line) configured over a portion of the gate line.

wherein

Claim 4:

- the storage metal layer formed with the data line on the gate insulation layer.

Claim 6:

- the data line, the source electrode 186, the drain electrode 178 and the storage metal layer (gate lines 162) are all formed of a double-layered metal pattern consisting of a lower part of molybdenum alloy (barrier layer 176a/178a) and an upper part of copper (Cu).

2. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Hwang et al. (US20040041958A1).

Hwang et al. teaches an array substrate for use in a liquid crystal display device comprising:

Claim 1:

- a gate electrode 131 and a gate line 133, each having a molybdenum alloy (Mo-alloy layer (first or barrier layer) and a copper (Cu) layer (second layer) configured sequentially on a substrate;
- a gate insulation layer 137 on the substrate to cover the gate electrode and the gate line;
- an active layer 139 arranged on the gate insulation layer in a portion over the gate electrode;
- an ohmic contact layer 141 on the active layer;
- a data line inherently on the gate insulation layer, the data line crossing the gate line and defining a pixel region;
- source and drain electrodes 149/151 on the ohmic contact layer, the source electrode inherently extending from the data line, and the drain electrode spaced apart from the source electrode;
- a passivation layer 159 on the gate insulation layer covering the data line and the source and drain electrodes, the passivation layer having a drain contact hole 182 exposing a portion of the drain electrode; and

- a pixel electrode 169 configured on the passivation layer in the pixel region, the pixel electrode electrically contacting the drain electrode through the drain contact hole.

Claim 3:

- a storage metal layer (157) configured over a portion of the gate line.

Wherein

Claim 2:

- the molybdenum alloy (Mo-alloy) layer includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof (claim 2 in Hwang et al. (US20040041958A1)).

Claim 4:

- the storage metal layer formed with the data line on the gate insulation layer.

Claim 5:

- the pixel electrode electrically contacts the storage metal layer via a storage contact hole.

Claims 6-7:

- the data line, the source electrode 149, the drain electrode 151 and the storage metal layer 157 are all formed of a double-layered metal pattern consisting of a lower part of molybdenum alloy 143 and an upper part of copper 145; wherein the molybdenum alloy (Mo-alloy) includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof (claims 6 and 7 in Hwang et al. (US20040041958A1)).

Claim 8:

- the data line, the source electrode, the drain electrode and the storage metal layer are all formed of a single layer of copper (claim 8 in Hwang et al. (US20040041958A1)).

Claim 9:

- the molybdenum alloy layer of the gate electrode and gate line has a thickness in a range from about 10 to about 500 angstroms (claim 9 in Hwang et al. (US20040041958A1)).

Claim 10:

- the copper layer has a thickness in a range from about 500 to about 5000 angstroms (claim 10 in Hwang et al. (US20040041958A1)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (US6468822B2) as applied to claim 1, in view of Ikeda et al. (US6323490B1).

Maeda et al. fail to disclose the gate lines made of stacked structure including the molybdenum alloy (Mo-alloy) layer includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof.

Ikeda et al. teach (col. 13 lines 52-58) the gate lines having stacked structure made of the molybdenum alloy (Mo-alloy) layer including one of tungsten (W) for allowing taper-etching the gate electrode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify an array substrate for use in a LCD device as Maeda et al. disclosed with the gate lines having stacked structure made of the molybdenum alloy (Mo-alloy) layer including one of tungsten (W) for allowing taper-etching the gate electrode, as taught by Ikeda et al. (col. 13 lines 55-56).

4. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (US6468822B2) as applied to claim 1, in view of Song (US6307602B1).

Maeda et al. further teach (Figs. 3 and 6) an array substrate with the data line (source line 22), the source electrode 7, the drain electrode 6 and the storage metal layer 2 all formed of a double-layered metal pattern consisting of a lower part of molybdenum alloy 1a/2a/6a/7a and an upper part of copper 1b/2b/6b/7b; wherein the molybdenum alloy (Mo-alloy) includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof (claims 6-7).

However, Maeda et al. fail to disclose the features of claims 3-5.

Song an array substrate for use in a LCD device with a storage metal layer 150 configured over a portion of the gate line (claim 3), formed with the data line on the gate insulation layer (claim 4), wherein the pixel electrode electrically contacts the

storage metal layer via a storage contact hole (claim 5) for maintaining the aperture ratio of the LCD (col. 3 lines 51-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify an array substrate for use in a LCD device as Maeda et al. disclosed with a storage metal layer 150 configured over a portion of the gate line (claim 3), formed with the data line on the gate insulation layer (claim 4), wherein the pixel electrode electrically contacts the storage metal layer via a storage contact hole (claim 5) for maintaining the aperture ratio of the LCD as taught by Song (col. 3 lines 51-52).

5. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (US6468822B2) as applied to claim 1, in view of Tanaka (US6393042B1).

Maeda et al. fail to disclose the features of claims 9-10.

Tanaka teaches the gate lines have double-film structures, wherein the molybdenum alloy layer (first conductive layer) of the gate electrode and gate line has a thickness in a range from about 5nm-50nm (50-500 angstroms), which is in a range of 10 to about 500 angstroms, and the copper layer (second conductive layer) has a thickness in a range from about 200-400nm (2000-4000 angstroms), which is in a range of 500 to about 5000 angstroms.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify an array substrate for use in a LCD device as Maeda et al. disclosed the gate lines having double-film structures, wherein

the molybdenum alloy layer (first conductive layer) of the gate electrode and gate line has a thickness in a range from about 5nm-50nm (50-500 angstroms), which is in a range of 10 to about 500 angstroms, and the copper layer (second conductive layer) has a thickness in a range from about 200-400nm (2000-4000 angstroms), which is in a range of 500 to about 5000 angstroms for lowering resistance of gate lines as taught by Tanaka (col. 23 lines 5-6).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Nakayama et al. (US 6404465 B1) disclose a liquid crystal display wherein storage electrodes overlap upper part of source lines and pixel electrodes overlap upper part of storage electrode.

Lee et al. (US 6686661 B1) disclose a thin film transistor having a copper alloy wire.

Kwon et al. (US 20010019375 A1) disclose a liquid crystal display device with gate line havinga double metal layer structure such as Mo/AlNd, Mo/Al or Cr/AlNd.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim H. Robert can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAN C. NGUYEN
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